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RITTER, LANG & KAPLAN 12930 SARATOGA AE. SUITE D1 SARATOGA, CA 95070			MOORE, IAN N	
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DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/872,141	Applicant(s) KATUKAM ET AL.	
	Examiner Ian N Moore	Art Unit 2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 10-13, 16, 17, 21-24, 28-36 and 39-42 is/are rejected.
- 7) ☒ Claim(s) 8, 9, 14, 15, 18-20, 25-27, 37 and 38 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1/02, 8/04, 10/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings, FIG. 1, are objected to because the link or path labels are not clearly visible. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1, 16 and 20 are objected to because of the following informalities: Appropriate correction is required.

Claim 1 recites, “a path” in line 1, and “a path” in line 10. For consistency, it is suggested to “a path” in line 10 to “the path” since it refers back to the same path identified in line 1.

Claim 16 recites, “the set of **network** elements” in line 25-26; however, this limitation is initially recited as “a set of elements” in line 25. Appropriate correction is required in order to be consistent. Claim 16 recites, “the plurality of **network** elements” in line 26; however, this limitation is initially recited as “a plurality of elements” in line 2. Appropriate correction is required in order to be consistent.

Claim 20 recites, “the second segment” in line 2. For clarity, it is suggested to change to “a second segment” since the limitation is reciting for the first time.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-7,10-13,16,17,21-24,28-32,33-36,39-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Finn (US 6,728,205).

Regarding Claim 1, Finn discloses a device (see FIG. 1, Network Node 12a) for creating a path (see FIG. 2, a path 34 or 36, see col. 18, lines 12-16; or see FIG. 4A, a path 92, see col. 22, lines 54-58) between a first element (see FIG. 2, Source node 30a, see col. 18,

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lines 15-17; or FIG. 4A, Source Node N1, see col. 22, lines 34-36) and a second element (see FIG. 2, Destination Node 30b, col. 18, lines 1-5; or FIG. 4A, Destination Node D1, col. 22, lines 35-37), the path being arranged to include a third element (see FIG. 2, Node 30c or 30i, col. 18, lines 4-10; or see FIG. 4A, N4, col. 22, lines 35-45), wherein the first element, the second element, and the third element are included in an optical network (see FIG. 1, network 10; see col. 8, lines 8-14; see col. 28, lines 63-67; SONET/SDH optical network), the device comprising:

a processor (see FIG. 1, a combined system of APS processor 14 and protection switching module 18; see col. 15, lines 15-20, 36-43); and

a storage device (see FIG. 1, Network Node 12a comprises a memory which stores the method to be executed), the storage device being arranged to store computer code (see col. 16, lines 36-47; network node comprises a memory to store computer/software instructions) for implementing a first mechanism (see FIG. 3, steps 58, 60; identifying/assigning and constructing a path) which causes the third element to be identified (see col. 20, lines 14-45; identifies/assigns node(s) in the path),

the storage device further being arranged to store computer code (see col. 16, lines 36-47; computer/software instructions) for implementing a second mechanism which causes a path between the first element and the second element to be computed such that the path traverses the third element (see FIG. 3, step 66 and 68; see col. 21, lines 4-40; computes and selects a path in between source and destination nodes in a first cycle of path via intermediate/upstream/downstream node(s)), wherein the processor processes the computer

codes (see col. 16, lines 36-47; the combined processor processes the computer/software instructions).

Regarding Claim 2, Finn discloses wherein the first element (see FIG. 2, Source node 30a, see col. 18, lines 15-17; or FIG. 4A, Source Node N1, see col. 22, lines 34-36) and the second element (see FIG. 2, Destination Node 30b, col. 18, lines 1-5; or FIG. 4A, Destination Node D1, col. 22, lines 35-37), and the third element are nodes (see FIG. 2, Node 30c or 30i, see col. 18, lines 4-10; or see FIG. 4A, N4, col. 22, lines 35-45).

Regarding Claim 3, Finn discloses wherein the first element (see FIG. 2, Source node 30a, see col. 18, lines 15-17; or FIG. 4A, Source Node N1, see col. 22, lines 34-36) and the second element are nodes (see FIG. 2, Destination Node 30b, col. 18, lines 1-5; or FIG. 4A, Destination Node D1, col. 22, lines 35-37), and the third element is a link (see FIG. 2, an arc 36a or 34a, col. 18, lines 4-10; or see FIG. 4A, a path 92a, col. 22, lines 54-64).

Regarding Claim 10, Finn discloses an apparatus (see FIG. 1, Network Node 12a) for creating a path (see FIG. 2, a path 34 or 36, see col. 18, lines 12-16; or see FIG. 4A, a path 92, see col. 22, lines 54-58) between a first element (see FIG. 2, Source node 30a, see col. 18, lines 15-17; or FIG. 4A, Source Node N1, see col. 22, lines 34-36) and a second element (see FIG. 2, Destination Node 30b, or FIG. 4A, Destination Node D1) in an optical network (see FIG. 1, network 10; see col. 8, lines 8-14; see col. 28, lines 63-67; SONET/SDH optical network), the path being arranged to include a third element (see FIG. 2, Node 30c or 30i; or see FIG. 4A, N4), the apparatus comprising:

a first means (see FIG. 1, a combined system of APS processor 14 and protection switching module 18; see col. 15, lines 15-20, 36-43; see FIG. 3, steps 58, 60;

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identifying/assigning and constructing a path) for identifying the third element (see col. 20, lines 14-45; identifies/assigns node(s) in the path); and

a second means (see FIG. 1, a combined system of APS processor 14 and protection switching module 18; see col. 15, lines 15-20, 36-43; see FIG. 3, step 66 and 68) for computing a path between the first element and the second element such that the path traverses the third element (see col. 21, lines 4-40; computes and selects a path in between source and destination nodes in a first cycle of path via intermediate/upstream/downstream node(s)).

Regarding Claims 4 and 11, Finn discloses wherein the first mechanism/means is arranged to identify the third element as being a component of the path (see FIG. 2, node 30c or 30i is part of the path, col. 18, lines 15-25; or see FIG. 4A, node N4 is part of the path 92; see col. 22, lines 34-55).

Regarding Claims 5 and 12, Finn discloses wherein the first mechanism is further arranged to identify a fourth element (see FIG. 3A, step 70, 72; see col. 21, lines 50-56; a node not covered by the first path, i.e., see FIG. 2, node 30h, 30c, or 30d) as being a component of the path (see FIG. 2, node 30 h, 30c, or 30d is a part of the path 36), the fourth element being arranged to be traversed after the third element is traversed (see FIG. 2, node 30 h, 30c, or 30d is traversed after node 30i is traversed; see col. 18, lines 13-25).

Regarding Claims 6 and 13, Finn discloses wherein the path (see FIG. 2, path 36) includes a plurality of segments (see FIG. 2, arc 36a-36i), and wherein the second mechanism is further arranged to compute a first segment (see FIG. 2, arc 36a) associated with the first element (see FIG. 2, source node 36a utilizes arc 36a) and the third element (see

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FIG. 2, intermediate node 30 i utilizes arc 36a), the first segment being included in the plurality of segments (see FIG. 2, arc 36a is included in arcs 36a-36i; see col. 18, lines 1-10, 45-50).

Regarding Claim 7, Finn discloses implementing a third mechanism (see FIG. 3A, step 70 and 72) which causes the fourth element (see FIG. 2, node 30h, 30c, or 30d) and the second element (see FIG. 2, destination node 30b) to be substantially prevented from being included as a part of the first segment (see FIG. 2, arc 36a; see col. 21, lines 50-59; see col. 22, lines 5-9; a next path (see FIG. 3A, step 72) includes nodes that are not already include in a first path (see FIG. 3A, step 66). Thus, destination node 30b and node 30h, 30c, or 30d are not included in the arc).

Regarding Claim 16, Finn discloses an apparatus (see FIG. 1, Network Node 12a) for routing a path (see FIG. 2, a path 34 or 36, see col. 18, lines 12-16; or see FIG. 4A, a path 92, see col. 22, lines 54-58) between a source node (see FIG. 2, Source node 30a, see col. 18, lines 15-17; or FIG. 4A, Source Node N1, see col. 22, lines 34-36) and a destination node (see FIG. 2, Destination Node 30b, or FIG. 4A, Destination Node D1) included within a network (see FIG. 1, network 10; see col. 8, lines 8-14; see col. 28, lines 63-67; SONET/SDH optical network), the network further including a plurality of elements (see FIG. 2, arcs 36a-36h and 34a-h), the apparatus comprising:

an identifier (see FIG. 12a, protection switching module 18 and APS processor 14 performs the identifying/assign step, see FIG. 3, steps 58, 60; identifying/assigning step) for identifying a set of elements (see FIG. 2, Node 30c, 30d, 30h, 30i and its arcs 36a-b, 36c-36e, 36h; or see FIG. 4A, N4) to be included in the path (see col. 20, lines 14-45;

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identifies/assigns node(s) and its associated arcs in the path between source and destination nodes), the set of network elements (see FIG. 2, Node 30c, 30d, 30h, 30i and its arcs 36a-b, 36c-36e, 36h; or see FIG. 4A, N4) being included in the plurality of network elements (see FIG. 2, nodes 30s and their arcs 36a-36h and 34a-h);

a blocker (see FIG. 12a, protection switching module 18 and routing table 16 performs step of not including the intermediate node(s) and their arcs initially (i.e. blocking), see FIG. 3A, step 68,70; see col. 21, lines 30-56) for blocking at least a first element (see FIG. 3A, the first path/arc (i.e. arc 36a)) included in the set of elements from being used in generating a first segment of the path (see FIG. 2, arcs 36 a-b); see col. 21, lines 30-56.

a path router (see FIG. 12a, protection switching module 18 performs the step of switching and routing, per FIG. 3, step 66 and 68; see col. 21, lines 4-40; assigning, selecting and routing over a arc between source and intermediate/upstream/downstream node(s)), the path router being arranged to generate the first segment such that the first segment includes the source node (see FIG. 2, node 30a) and a second element (see FIG. 2, arc 36c), the second element being included in the set of elements (see FIG. 2, Node 30c, 30i, and their arcs 36a-b, 36c-36e, 36h), wherein the first segment does not include the first element (see FIG. 2, arc 36a-b does not include arc 36a since the second cycle/path along include intermediate nodes and its associated arc not already included in the first path).

Regarding Claim 17, Finn discloses wherein the blocker blocks substantially all elements included in the set of elements except for the second element (see FIG. 2, arc 36c) from being used in generating the first segment of the path (see FIG. 3A, step 68,70; see col. 21, lines 30-56; all nodes and its associated arcs which are already included in the first path

are not used expected, thereby, using the remaining intermediate nodes and its associated arcs (i.e. arc 36c) which are included in the path).

Regarding Claim 21, Finn discloses a method (see FIG. 3 and 3A, a method) for computing a circuit path (see FIG. 2, a path 34 or 36, see col. 18, lines 12-16; or see FIG. 4A, a path 92, see col. 22, lines 54-58) between a source node (see FIG. 2, Source node 30a, see col. 18, lines 15-17; or FIG. 4A, Source Node N1, see col. 22, lines 34-36) and a destination node (see FIG. 2, Destination Node 30b, col. 18, lines 1-5; or FIG. 4A, Destination Node D1, col. 22, lines 35-37) of an optical network (see FIG. 1, network 10; see col. 8, lines 8-14; see col. 28, lines 63-67; SONET/SDH optical network), the method comprising:

identifying at least a first element (see FIG. 2, Node 30c, 30i, or link 36a; or see FIG. 4A, N4; see FIG. 3, steps 58, 60; identifying/assigning nodes) that is to be traversed by the circuit path between the source node and the destination node (see col. 20, lines 14-45; identifies/assigns node(s) in the path between source and destination nodes); and

routing a first segment automatically (see FIG. 2, arc 34a or arc 36a-b; or see FIG. 4A, arc 92a), the first element being a part of the circuit path (see FIG. 2, node 30c or 30i is part of the path 34 or 36; or see FIG. 4A, node N4 is part of the path 92), wherein when the first element is a node (see FIG. 2, node 30c; or see FIG. 4, Node N4), the source node (see FIG. 2, source node 30a; or see FIG. 4A, source node N1) and the first element are components of the first segment (see FIG. 2, node 30c or 30i is part of arc 34a or 36a path; or see FIG. 4A, node N4 is part of the arc 92a); see FIG. 3, step 66 and 68; see col. 21, lines 4-40; the method assigns, selects and routes over a arc between source and intermediate/upstream/downstream node(s).

Regarding Claim 33, Finn discloses a computer program product (see FIG. 1, Network Node 12a) for computing a circuit path (see FIG. 2, a path 34 or 36, see col. 18, lines 12-16; or see FIG. 4A, a path 92, see col. 22, lines 54-58) between a source node (see FIG. 2, Source node 30a, see col. 18, lines 15-17; or FIG. 4A, Source Node N1, see col. 22, lines 34-36) and a destination node (see FIG. 2, Destination Node 30b, col. 18, lines 1-5; or FIG. 4A, Destination Node D1, col. 22, lines 35-37) of an optical network (see FIG. 2, Destination Node 30b, or FIG. 4A, Destination Node D1), the computer program product comprising:

computer code that causes at least a first element (see FIG. 2, Node 30c or 30i; or see FIG. 4A, N4) that is to be traversed by the circuit path between the source node and the destination node to be identified (see FIG. 3, steps 58, 60; see col. 20, lines 14-45; identifies/assigns node(s) (i.e. 30c, 30i, or N4) in the path between source and destination nodes);

computer code that causes a first segment to be routed (see FIG. 2, arc 34a or arc 36a; or see FIG. 4A, arc 92a), the first segment being a part of the circuit path (see FIG. 2, node 30c or 30i is part of the path 34 or 36; or see FIG. 4A, node N4 is part of the path 92; see col. 18, lines 15-25; see col. 22, lines 55-67), wherein when the first element is a node (see FIG. 2, node 30c; or see FIG. 4, Node N4), the source node and the first element are components of the first segment (see FIG. 2, node 30c or 30i is part of arc 34a or 36a path; or see FIG. 4A, node N4 is part of the arc 92a); see FIG. 3, step 66 and 68; see col. 21, lines 4-40; the method assigns, selects and routes over a arc between source and intermediate/upstream/downstream node(s); and

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a computer-readable medium (see FIG. 1, Network Node 12a comprises a memory) that stores the computer codes (see col. 16, lines 36-47; the memory stores the computer/software instructions to be executed).

Regarding Claims 22 and 34, Finn discloses wherein routing the first segment automatically includes routing the first segment automatically using a shortest path first algorithm (see col. 22, lines 24-27).

Regarding Claims 23, 31, and 35, Finn discloses identifying a second element (see FIG. 3A, step 70, 72; see col. 21, lines 50-56; a node or arc not covered by the first path; a node i.e., see FIG. 2, node 30h, 30c, or 30d; or its associated arcs 36e-h or 36b-c) that is to be traversed by the circuit path between the first element and the destination node (see FIG. 2, node 30 h, 30c, or 30d (or its associated arcs 36e-h or 36b-c) is traversed after node 30i is traversed; see col. 18, lines 13-25); and

blocking the second element from being available for use in routing the first segment automatically (see FIG. 3A, step 68,70; see col. 21, lines 30-56; the first path/arc (i.e. arc 36a) does not automatically include an intermediate node (i.e. node 30h, 30c, or 30d) or its associated arcs (36e-h or 36b-c), thereby blocking/not-already-including the intermediate node), wherein routing the first segment automatically includes routing the first segment to substantially avoid including the second element as a component (see col. 21, lines 50-56; routing arc 36a from the source node 30a does not automatically include (i.e. avoid including) the intermediate node (i.e. node 30h,30c, or 30d; or, arcs 36e-h or 36b-c)).

Regarding Claims 24, 32 and 36, Finn discloses blocking the destination node from being available for use in routing the first segment automatically (see FIG. 3A, step 68,70;

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see col. 21, lines 30-56; the first path/arc (i.e. arc 36a) does not automatically include the destination node (i.e. node 30b), thereby blocking/not-already-including the node), wherein routing the first segment automatically further includes routing the first segment to substantially avoid including the destination node as a component (see col. 21, lines 50-56; routing arc 36a from the source node 30a does not automatically include (i.e. avoid including) the destination node 30b).

Regarding Claims 28 and 39, Finn discloses wherein when the first element is a first link (see FIG. 2, arc 36a-36b), the method further includes: identifying an initial node of the first link (see FIG. 2, Node 30i identifies and connects to an arc 36a; see col. 20, lines 14-45).

Regarding Claims 29 and 40, Finn discloses wherein routing the first segment automatically includes routing the first segment (see FIG. 2, arc 34a or arc 36a; or see FIG. 4A, arc 92a) from the source node (see FIG. 2, source node 30a) to the initial node of the first link when the first element is the first link (see FIG. 2, route to node 30i when arc 36a is the first arc; see col. 21, lines 4-40).

Regarding Claims 30 and 41, Finn discloses routing a second segment automatically (see FIG. 2, a combined arcs 36b, 36c, 36e, and 36h between Node 30i and destination node 30b), wherein the first link is included in the second segment (see FIG. 2, arc 36b is included in the combined arcs; see FIG. 3, step 66 and 68; see col. 21, lines 4-40).

Regarding Claim 42, Finn discloses wherein the computer-readable medium is one selected from the group consisting of a hard disk, a CD-ROM, a DVD, a computer disk, a tape drive, a computer memory and a data signal embodied in a carrier wave (see FIG. 1,

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Network Node 12a comprises a computer memory which stores the method to be executed; see col. 16, lines 36-47).

Allowable Subject Matter

5. Claims 8,9, 14,15,18-20,25-27, 37 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 571-272-3085. The examiner can normally be reached on M-F: 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gnm

2/1/05


BOB PHUNKULH
PRIMARY EXAMINER